May1625

Latent Damage and Reliability in Semiconductor Devices

DESIGN DOCUMENT

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1. Summary

This design document includes a detailed description of our Senior Design Project. We will be discussing our project timeline, the system level design, and also a detailed system breakdown.

1.1 Abstract

Latent damage due to an Electrostatic Discharge (ESD) event is a topic of debate within the Semiconductor industry. Our goal, as a team, is to research if latent damage does or does not exist within semiconductor devices after experiencing an ESD event. Our next task is to conclude whether these devices are reliable after proving latent damage exists. Section 3 and 4 will explain how the research will be conducted.

1.2 Background

1.2.1 Previous Work Completed

Xuan Zhang, a student who was previously performing this research for Dr. Geiger had a similar goal to ours. She had designed a few Printed Circuit Boards (PCBs) and left those for us to utilize. These boards held two different purposes. One design was going to be used to induce an ESD event on a device. The other design is to be used to monitor multiple devices while accelerating their lifetime. More details about the PCBs and how we will be using them can be found in Sections 3.2.1, 4.1.1, and 4.2.1.

1.3 Hypothesis

As a team we expect that if an ESD event occurs on a semiconductor device, then latent damage exists. Furthermore, this latent damage can cause the reliability of these devices to decrease; resulting in the Mean Time to Failure (MTTF) to be substantially shorter than the manufacturing specification.

2. Project Timeline

2.1 Summary

In *Figure 1*, the project highlights and multiple key components have been listed to help manage our time as a team. This schedule will be followed strictly but also adjusted accordingly throughout both semesters of Senior Design. A project timeline is the most important aspect to a design document and should be taken seriously if success is desired.

2.2 Gantt Chart

	Task Name	Start Date	End Date	% Complete
1				
2				
3	**Fall 2015 Semester**	**08/24/15**	**12/16/15**	**36%**
4	Project Assignments	08/25/15	09/01/15	100%
5	Research	09/01/15	10/07/15	100%
6	Website	09/16/15	09/30/15	100%
7	Project Plan v1	09/30/15	10/02/15	100%
8	Order Parts	10/07/15	10/19/15	80%
9	Design Document v1	10/20/15	10/23/15	30%
10	Create Test System	10/26/15	11/06/15	10%
11	DUT Functionality Test Boards			
12	ESD Stressing System			
13	Verify Test System Functionality			
14	Test Samples of Devices	11/06/15	11/25/15	
15	Prepare Presentation	11/25/15	12/14/15	
16	Presentation of Implementation	12/14/15	12/16/15	
17	**Spring 2016 Semester**	**01/11/16**	**04/29/16**	
18	Multiple Sample Tests	01/11/16	02/08/16	
19	Repeat until Desired Failure Rate			
20	Record Data			
21	Data Analysis	02/08/16	02/22/16	
22	Redesign Test System	02/22/16	02/29/16	
23	Repeat Sample Tests	02/29/16	03/28/16	
24	Data Analysis	03/28/16	04/04/16	
25	Verify Hypothesis	04/04/16	04/11/16	
26	Prepare Presentation	04/11/16	04/27/16	
27	Final Presentation	04/27/16	04/29/16	

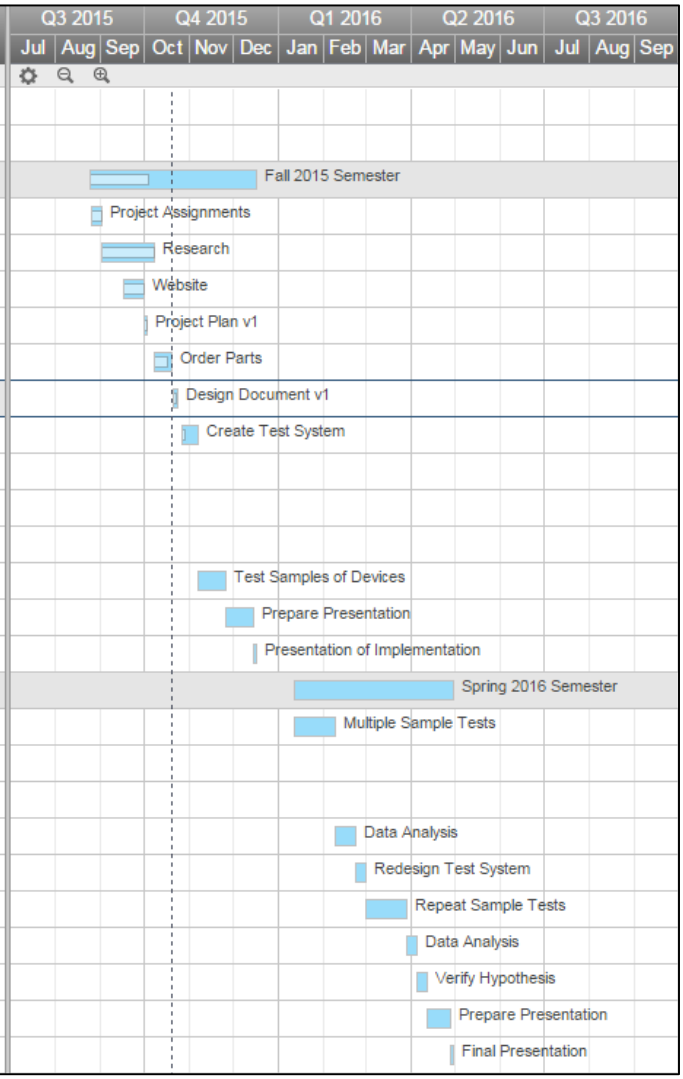

Figure 1: Gantt chart for Project
(Updated on October 20th, 2015)

3. System Level Design

3.1 Summary

Our team has a goal to design and run an experiment to show whether or not latent damage exists in Commercial off-the-Shelf (COTS) semiconductor devices after an ESD event has occurred. Specifically, our device of interest is a CMOS hex inverter (CD4049UBE) manufactured by Texas Instruments using a bulk-CMOS process.

Latent damage is the type of damage that cannot be measured through the devices electrical characteristics, but a physical defect is present and as a direct result, the device's lifetime is reduced. This kind of phenomenon would mean that our COTS devices can have unforeseen reliability issues, which in turn could mean that present repair procedures (i.e. swapping out boards on a failed system until the functionality returns) for any system undergoing stress could be invalid.

Our primary interest in this project is to electrically stress a large sample of a COTS device by ESD and measure the failures versus expected lifetime of the devices.

3.2 Test Equipment

3.2.1 ESD Stress PCB & DUT burn-in PCB

The ESD Stress PCB is designed to charge a capacitor (*Figure 2*), via a high-voltage source, and then by flipping a switch, discharge that capacitor to the Device under Test (DUT). This will allow us to simulate an ESD event on a device. Currently, the high-voltage source on the existing board is non-functional due to a previous experiment. Our plan is to use a standalone high-voltage source as an alternative. A more detailed description of this PCB can be found in Section 4.1.1.

Figure 2: ESD Stress PCB

The DUT burn-in PCB (*Figure 3*) is used to monitor multiple devices while accelerating their lifetime in a burn-in oven. It has a set of Light-Emitting Diode (LED) arrays which provide output levels of the devices as well as a control switch to vary the input level of the devices. A more detailed description of this PCB can be found in Section 4.2.1.

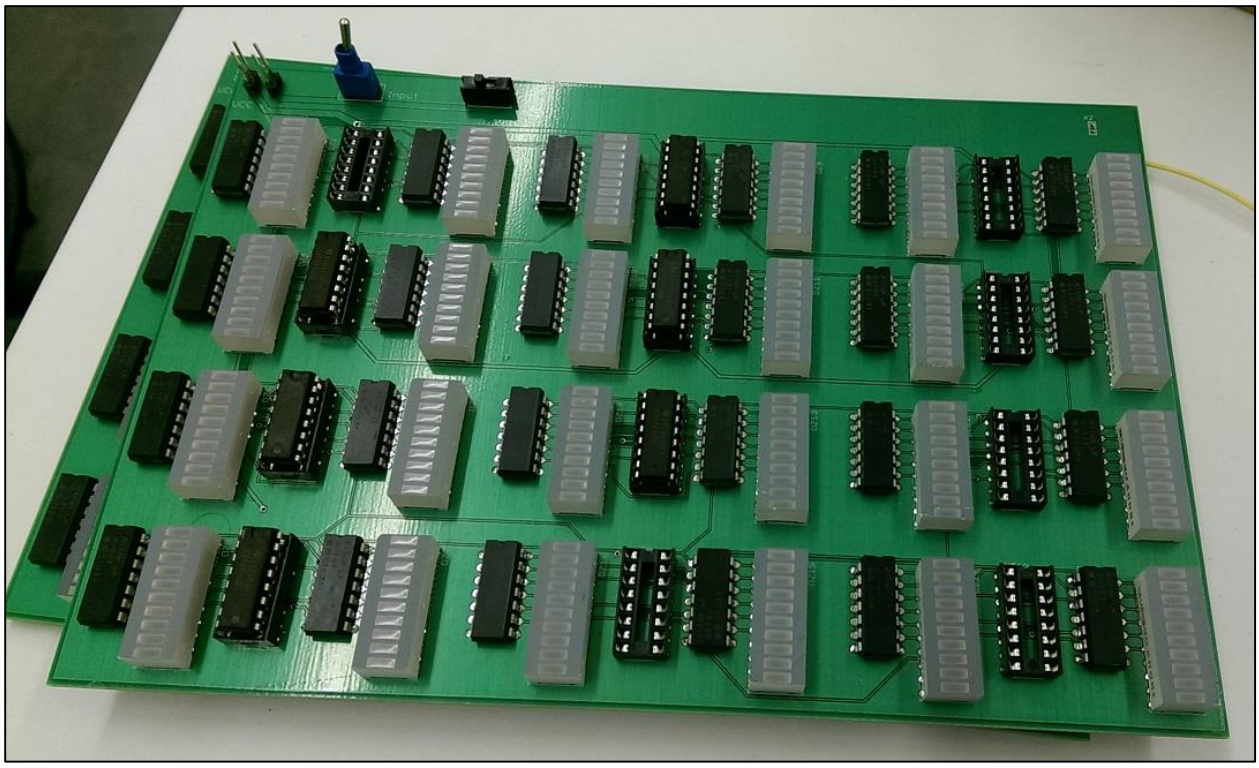

Figure 3: DUT burn-in PCB

3.2.2 Burn-in Oven

The point of our experiment is to complete it before graduating. Under normal circumstances, the expected lifetime for a COTS device is on the order of decades.

But as it is well known, a device under operation at a particularly high temperature will experience an accelerated lifetime. To allow the experiment to be completed on the order of months, we will use a burn-in oven to accelerate our parts' remaining lifespan after the ESD stress.

From there, we can measure the devices and record how much longer they last *after* the burn-in.

3.3 Testing Procedure

Much of the testing procedure has already been detailed. However, in the interest of completeness and usability of this document, our current plan for testing is detailed here.

3.3.1 ESD Stress

The first part of our experiment will involve taking a sample of 100 parts, subjecting them to a high-voltage ESD event, using the PCB as described in Section 3.2.1 of this document. A capacitor will be charged with a high-voltage source, then discharged into the input gates of each COTS part.

During this type of ESD event, all outputs will be tied low (ground) to put the pMOS transistors in a high-current mode which ultimately induces more stress on the device by raising temperatures.

3.3.2 Accelerated Lifetime

Once the devices have been stressed, they will be inserted into a burn-in oven to accelerate their lifetime. As mentioned in Section 3.2.2, this will accelerate the overall lifetime of our device to much shorter, manageable durations. Keep in mind that the devices will need to be powered-on and kept in the high-current mode during this testing. By doing this, we can complete the project in months rather than years.

3.3.3 Pass & Fail Conditions

After the burn-in, the statistic of interest in the devices is how much longer they last after the stressing and accelerated lifetime.

Our metric for determining failure of the device will be through the logic levels. As each device contains multiple inverters, the status of the LED indicators on the DUT burn-in PCB should be opposite that of the shared input of the testing board. A failure will be considered when any of the inverters on a device have incorrect logic.

The truth table of a single inverter is shown in *Figure 4*. If at any time an inverter has an incorrect logic level, then the device has failed. At which point, the failing inverter and device lifetime will be recorded for later analysis.

Figure 4

Input	Output
0	1
1	0

Given this, it will also be worth noting *how* the device failed. Is the device always giving a high output? Is the device always giving a low output? Or is it giving reverse operation? Which one of these three possible outcomes occurs for failed devices might also be worthwhile to study for our project. If a pattern emerges, it may suggest that the pull-up network (PUN) or pull-down network (PDN) of COTS devices are more vulnerable to ESD events and latent damage. If so, this may have further implications for future studies and preventative measures.

3.4 Data Analysis

Just collecting raw data isn't enough to draw a conclusion. Statistical analysis must be performed to make a conclusion about our results.

3.4.1 Mean Time to Failure (MTTF)

The basis for determining the existence (or non-existence) of latent damage is through the mean lifetime of the parts, or the Mean Time to Failure (MTTF).

As it may be obvious, a higher MTTF in our sample (as compared to a control group) would be counter-intuitive. This would imply that the ESD event actually *helped* our COTS part last longer! What we're expecting, should latent damage exist, is for the sample's MTTF be lower than our control groups'.

3.4.2 Statistical Analysis

However, just having a lower MTTF isn't enough to conclude that our devices actually have latent damage that was caused by the ESD stress.

Because of the nature of semiconductors, we cannot say with 100% certainty that our sample was valid. Due to variance in any manufacturing process, some devices will last an exceptionally long amount of time, while others will fail immediately. We must use statistical testing to generate a high confidence level of our MTTF being lower.

The sample size of 100 is large enough for us to apply the Central Limit Theorem, which will allow us to treat the sample as a Normal Distribution. From there, it's a matter of using procedures from statistics courses.

We'll start with a hypothesis and calculate a P-value based off of it. From that P-value, we can possibly reject the hypothesis or confirm it with a certain confidence level. Just like the nature of nature, we cannot say anything with certainty. But a statistically significant result one way or the other will allow us to make a conclusion.

3.5 Safety Concerns

Safety during this experiment is definitely of great importance. The dangers to us during experimentation are the high temperatures of the burn-in oven and the high-voltages used to perform the ESD stress.

The current plan is to use a commercial electric fencer to produce the high-voltages. However, it can't be expected that the fencer will be able to output high amounts of *energy*. Still, the higher voltage will be a much nastier shock than what we normally get from our usual lab equipment.

The burn-in oven also could pose burn hazards, but still shouldn't be potentially lethal under ordinary circumstances. After placing boards in the burn-in oven for a desired amount of time, we will need to use heat-resistant mitts to handle the boards and devices.

3.6 Advantages & Disadvantages

There are, of course, advantages and disadvantages of our experimental approach.

If latent damage is found, it can be found valid only for COTS devices, specifically hex inverters. This can be seen as an advantage or disadvantage.

Another disadvantage of our approach is that we also are not looking at the electrical properties of the devices. While latent damage shouldn't have an impact on the electrical properties of the DUT, there could still be non-latent damage we weren't measuring.

However, this approach does give us advantages. The test structure doesn't need to be designed from scratch. Further, we also have a rather simple procedure for the measurements and data analysis.

3.7 Block Diagrams

Figure 5 shows the different system level block diagrams that our project encompasses. There are three distinct sections to our project: ESD Stress, Accelerate Lifetime, and Data Analysis.

Within the ESD Stress block there are two sub-blocks: Stress DUTs and Check Functionality. Approximately 200 devices will be stressed by simulating an ESD event. Then, the functionality of each device will be checked and recorded; we are shooting for a 50% failure rate.

Following ESD Stress, the Accelerate Lifetime block contains three sub-blocks: Test 50% of Stressed DUTs, Burn-in DUTs, and Check Functionality. The devices that passed the first functionality check will be used as our sample (approximately 50%). Next, the burn-in oven will be used to accelerate their lifetime. While in the burn-in oven, functionality will be checked at a desired interval. We will continue to check the functionality until 100% of the devices have failed.

Lastly, after all of the devices have failed and the burn-in step has been completed, we will move onto our last block, Data Analysis. We will be performing statistical calculations and hopefully verifying our original hypothesis.

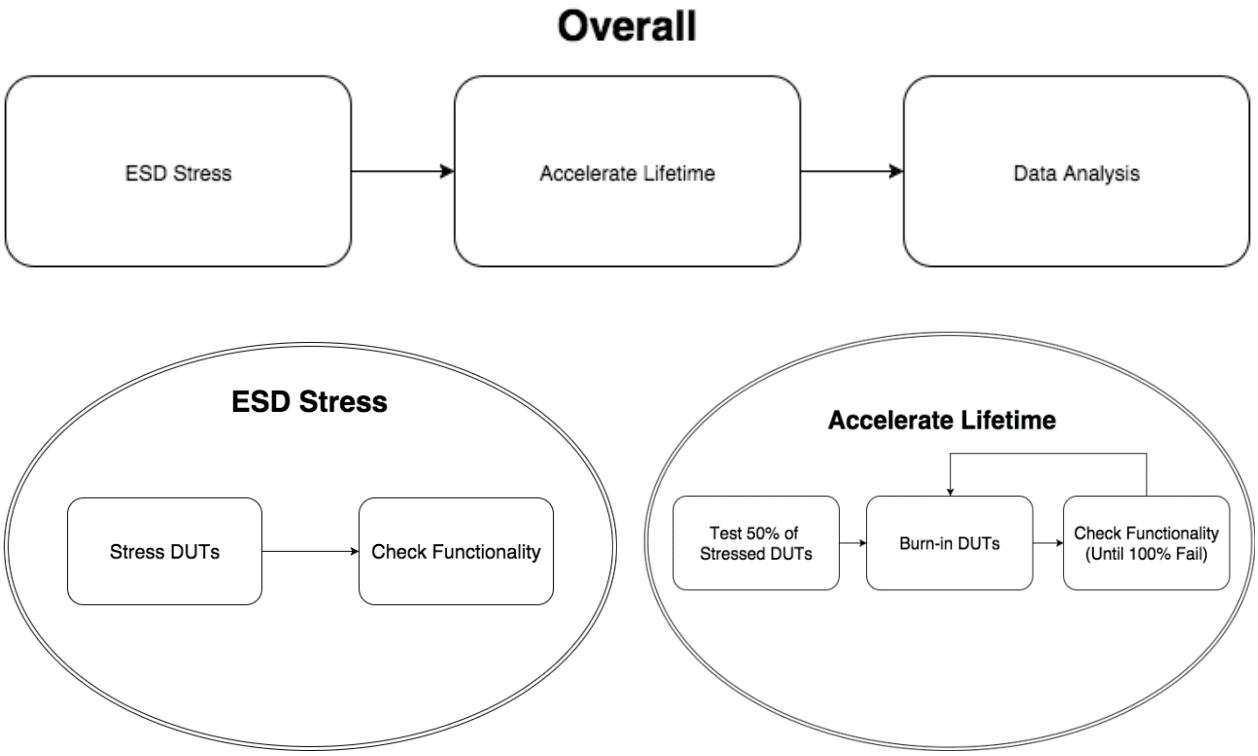

Figure 5: System Level Block Diagrams

4. Detailed System Breakdown

4.1 ESD Stress System

The ESD Stress System is the mechanism and procedure that our group will use to hopefully inhibit latent damage in the COTS semiconductor devices. This system contains the ESD Stress PCB and the ESD Stress Procedure, both of which are detailed in Sections 4.1.1 and 4.1.2 respectively.

4.1.1 ESD Stress PCB

The ESD Stress PCB will be used to stress CMOS hex inverters (CD4049UBE) manufactured by Texas Instruments using a bulk-CMOS process, which contain six individual inverters in each package.

Stressing the devices (detailed in Section 4.1.2) is based off of the Human Body Model (HBM). Our approach is to charge a 100pF capacitor with a couple of kilovolts (kV). This capacitor is charged by a high-voltage source. After the capacitor is completely charged, it can then be discharged by the flip of a switch into the DUT, causing the ESD event to occur.

Our high-voltage source is intended for agricultural purposes, and as such, the cost is minimal. It's possible to obtain a programmable lab-grade high-voltage source, but due to the very low demand in the market, doing so would be expensive.

The output of our high-voltage source is a voltage of 8.5kV, but only for 1/4000 of every second. Therefore during the charging phase of the stressing procedure a set of diodes must be used to prevent any reverse current from flowing out of the capacitor when the output of the source is low. As always, there needs to be a resistor in series with these diodes to ensure that the voltage drop across each diode doesn't exceed the maximum specification of the devices. These diodes also must be able to withstand a particularly high reverse voltage without experiencing breakdown. Our design has specified diodes that can withstand a reverse bias of 4kV. Four of these diodes are being used to safely prevent capacitance charge loss.

Furthermore, the voltage of our source is higher than needed, and as such the voltage must be stepped down through the use of a simple voltage divider. Doing this allows us to further control what size voltage is used to stress the devices.

LED arrays on the PCB also allow a stressed part to be checked for immediate failure. The voltage being applied to the DUT could very well cause catastrophic damage. The goal of our experiment is to check for latent damage, not catastrophic damage. As such, non-working devices will be immediately discarded instead of studied in accelerated lifetime testing.

A schematic of the ESD stressing circuitry is shown in *Figure 6*.

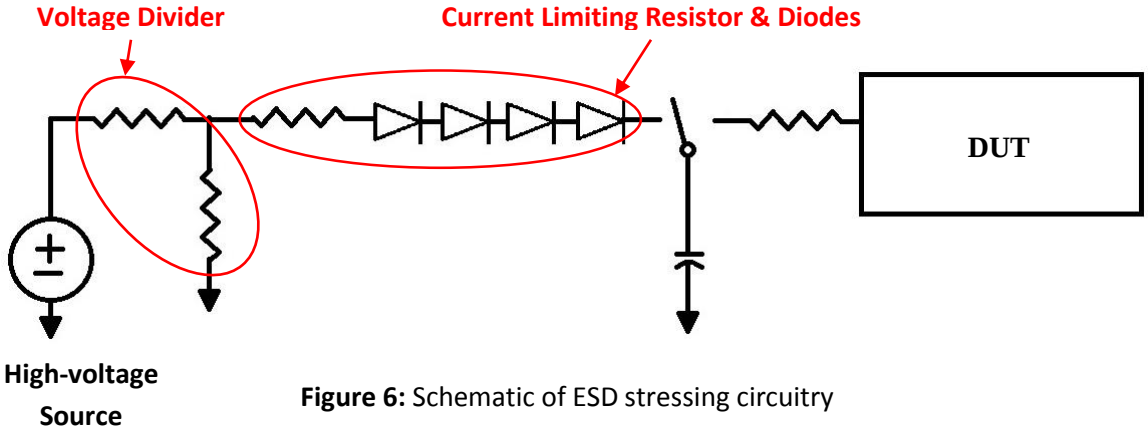

Figure 6: Schematic of ESD stressing circuitry

4.1.2 ESD Stress Procedure

The procedure by which to stress the devices can be partially understood through the previous section. However, for the usability of this document and the completeness of this section, it is detailed here.

The switch shown on the previous page is set to the high voltage side, to charge the capacitor to the desired voltage, set by the voltage divider's intentionally selected resistance values and the voltage drops across the diodes. This is the charging phase of the procedure.

During this charging phase, the device to be stressed is inserted into the board's stressing mechanism. Once the capacitor is given sufficient time to charge (which can also be determined through intelligent selection of resistor values) the switch is then flipped to discharge the capacitor through the device.

Once the device is "fully" discharged (given enough time for the RC circuit to mostly undergo most of its discharging), the device is then taken into the testing phase. Once again, the resistor values can be intelligently chosen to make the "sufficient time" short enough to cause a quick ESD event to occur.

The device is now stressed and must be tested before it can be used in our sample. Given the nature of the damage we are looking for, any device that has a failure cannot be used for our study. This testing phase is performed on the same PCB. A set of LED arrays are used to test each gate of the DUT.

This stressing procedure is further to be used to determine what level of voltage we should use to stress the devices. Different experimentally determined stress conditions have been suggested, one of which was to stress until roughly half of the stressed parts fail. Given this, the remaining parts can be tested for latent damage by accelerating their lifetime until failure. This type of system is described in Section 4.2.

4.2 Accelerated Lifetime System

The Accelerated Lifetime System is the mechanism and procedure that our group will use to accelerate the lifetime of the COTS semiconductor devices while testing for logical functionality along the way. This system contains the DUT burn-in PCB and the DUT burn-in Procedure, both of which are detailed in Sections 4.2.1 and 4.2.2 respectively.

4.2.1 DUT burn-in PCB

The DUT burn-in PCB can be populated with twelve CMOS hex inverters (CD4049UBE). There are 24 LED arrays on the PCB: one pair of LED arrays will show both the input and output of each inverter on the DUT. There are two sets of header pins at the top-left of the PCB as shown in *Figure 3*. The supply voltage for the DUT's and circuitry on the PCB can be applied to these headers. To control the supply voltage, the blue switch to the right of the headers can be flipped. To control the DUT output voltage, the other switch can be used.

4.2.2 DUT burn-in Procedure

According to a COTS manufacturer specification, our DUTs are expected to last a couple of decades under *normal* operating conditions. To significantly decrease the lifetime of a COTS device, temperature can be increased to a level that is outside of the *normal* operating conditions.

As previously explained, we will use a burn-in oven to accelerate our parts' remaining lifespan after the ESD stress. This means that the DUTs will be powered on within the burn-in oven and placed in a high-current mode (to further increase the temperature). Functionality will be checked at a given time interval to determine if and when a DUT has failed. The failures and respective time in the oven will then be recorded until 100% of the devices have failed. The data from each sample of approximately 100 devices can be used to analyze if latent damage exists in COTS semiconductor devices or not.

5. Bill of Materials

In *Figure 7* you will find our most updated copy of the Bill of Materials. This table includes all of the parts and components we will need to purchase or have already purchased in order to successfully complete our experiment and research. Our total project cost cannot exceed $1,200 – as defined in the proposal.

Bill of Materials					*Updated October 23rd, 2015*	
Item	**Qty.**	**Reference**	**Cost**	**Part Description**	**Supplier**	**Supplier #**
1	1	A66C	$39.99	Agway Electric Fencer (High-voltage source)	Zareba	A66C
2	25	GI250-4-E3/54	$8.85	4kV V_R Diodes	Digi-Key	GI250-4-E3/54GICT-ND
3	10	DHRB34A101M2BB	-	Murata Ceramic Disc Capacitors 100pF +/-20%	Mouser	81-DHRB34A101M2BB
4	500	CD4049UBE	-	TI Hex Inverters	Digi-Key	296-2055-5-ND
5	2	Custom	-	ESD Stress PCB	-	-
6	10	Custom	-	DUT burn-in PCB	-	-

Figure 7: Bill of Materials

6. Conclusion

After conducting our research we hope to have either proved or disproved our hypothesis. We will have successfully completed our experiments in a safe manner and will have stayed within our desired budget.

The semiconductor industry may disapprove of our research if we conclude that latent damage does indeed exist. Latent damage existing after an ESD event within a COTS device would decrease the reliability. This decrease in reliability might push the functionality of the device outside of the manufacturers' specifications, which could lead to undesirable profit loss.

There are many opportunities of growth for this type of research on semiconductor devices. We have simply performed a small portion on a specific COTS device and hope to encourage others to do the same.